Quad 2-input NAND 30Ω line driver (open collector) 74F3038

FEATURES

- 30Ω line driver
- 160mA output drive capability
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V_{CC} and GND when both side pins are used

DESCRIPTION

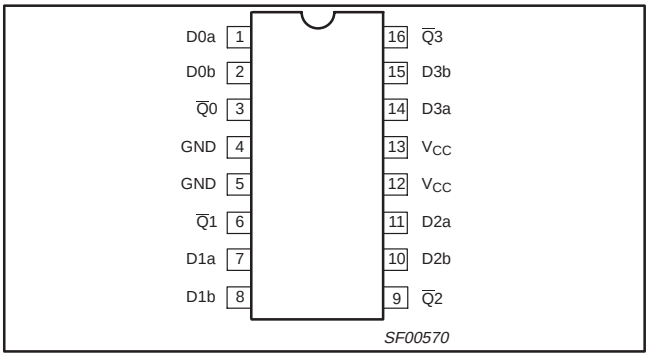
The 74F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50pF capacitance, a 500Ω pull-up resistor and a 500Ω pull-down resistor. (See Test Circuit).

Reducing the load resistors to 100Ω will decrease the t_{PLH} propagation delay by approximately 50% while increasing t_{PHL} only slightly. The graph of typical propagation delay versus load resistor (see AC Characteristics section for Graph) shows a spline fit curve from four measured data points, R_L = 30Ω, R_L = 100Ω, R_L = 300Ω, and R_L = 500Ω.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	6.0ns	17mA

ORDERING INFORMATION

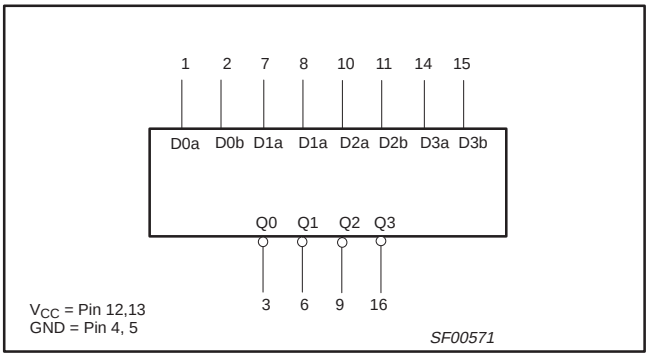
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F3038N	SOT38-4
16-pin Plastic SOL	N74F3038D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

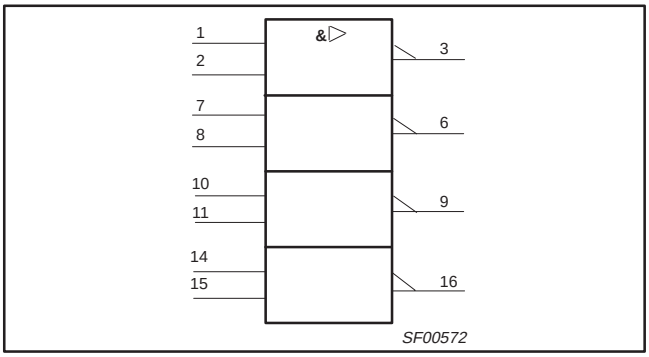
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$n	Data outputs	OC/266	OC/160mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state. OC = Open Collector.

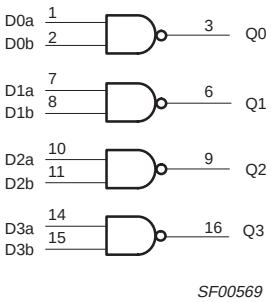
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 12,13
GND = Pin 4, 5

FUNCTION TABLE

INPUTS		OUTPUT
Dna	**Dnb**	**$\overline{Q}$n**
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10% V_{CC}		0.42	0.55	V
			I_{OL} = 160mA[3]	±5% V_{CC}			0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		3.5	6.0	mA
		I_{CCL}		V_{IN} = 4.5V		30	40	mA

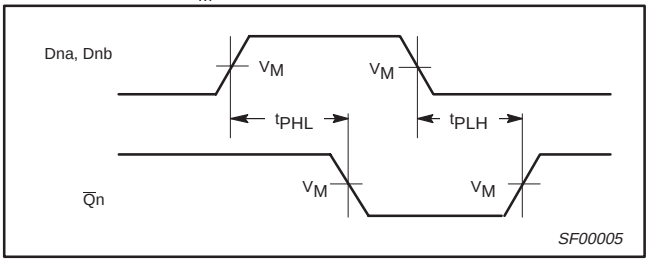
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	6.0 1.0	8.5 2.0	11.5 5.0	6.0 1.0	12.0 5.0	ns

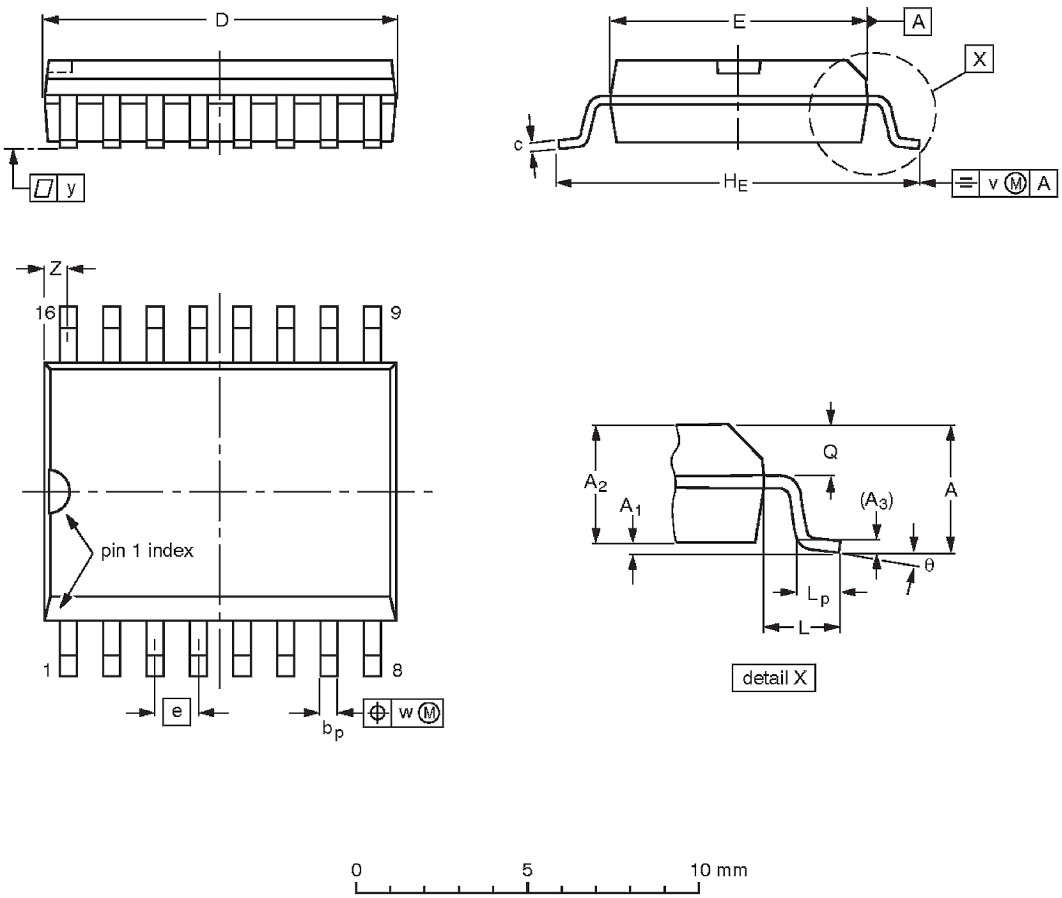
AC WAVEFORMS

For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Inputs to Output

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				